REMARKS

The Examiner has allowed claims 2-27 and 29-45 of the present application. Claims 1, 28, and 46-58 have been canceled. In this Amendment, new claims 59-68 are added.

New claims 59-68 are added in this Amendment. Support for claims 59-68 is provided in the specification by Figure 1 and pages 6-10 of the specification. Claims 59-68 are directed to features of the invention not emphasized in the claims presented thus far.

Claim 59 recites "a first memory block coupled to receive the address from the first register; and a second memory block coupled to receive the address from the second register." Further, claim 59 recites that "a first register that receives and stores an address on a first transition of a clock signal; a second register that receives and stores the address from the first register on a second transition of the clock signal." These features are not taught in the prior art references.

The Examiner has stated that Ryan (U.S. Pat. No. 5,749,086) teaches "at least two memory blocks, as shown in item 105 of figure 3." *See, e.g.,* Office Action mailed on December 9, 2003. However, Ryan does not teach "at least two memory blocks each of which is capable to be accessed at said address" as is recited, for example, in claim 14. Further, Ryan does not teach "a first memory block coupled to receive the address from the first register; and a second memory block coupled to receive the address from the second register." as is recited in new claim 59.

Ryan teaches a standard memory array that, as shown in Figure 3, is a 2048 by 1024 array of 8-bit words. The memory array shown in Figure 3 does not illustrate memory blocks at all. As is taught by Ryan, "[t]he memory array 101 includes a plurality of memory cells (not shown) arranged in rows and columns." (Ryan, col. 4, lines 55-57). Ryan further teaches that "[i]n one embodiment of the invention, the memory device 100 has an 8-bit word width -- meaning that to each specified memory address (combined row and column address) there is a one-to-one correspondence with 8 memory cells in the array 101." (Ryan, col. 4, lines 57-61). Therefore, Ryan does not teach memory blocks as has been suggested by the Examiner.

Claim 59 is allowable over the art cited in the Application. Claims 60-68 depend from claim 59 and are therefore allowable for at least the same reasons as is claim 59.

CONCLUSION

Applicants have amended the claims so that claims 2-27 and 29-45 are in condition for allowance. The remaining pending claims, claims 1, 28, 46-55, 57, and 58 have been canceled. New claims 59-68 have been added. Applicant respectfully requests that the Examiner enter the current amendments and timely issue a Notice of Allowance for claims 2-27, 29-45, and 59-68. If the Examiner contemplates a different action, the Examiner is invited to contact the Applicant's representative by phone at 650-849-6622 or by e-mail at gary.edwards@finnegan.com.

Please grant any extensions of time required to enter this response and charge any additional required fees to our Deposit Account No. 06-0916.

Respectfully submitted,

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Dated: June 24, 2004

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